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Result # 1 Relevance: ○○○○○

Method for the dynamic prediction of nonsequential memory accesses

25-Sep-2002 IPCOM000009888D English (United States)

Disclosed is a method for a software mechanism for the dynamic prediction of nonsequential memory accesses. Benefits include improved performance.

Result # 2 Relevance: ○

Multiple Channel Data Descriptor Prefetch Mechanism

1994-05-01 IPCOM000112360D English (United States)

Disclosed is a method for limiting the number of Peripheral Component Interconnect (PCI) bus arbitration cycles for a PCI Streamer family adapter when fetching transmit and receive descriptors. Streamer family adapters rely on data descriptors in host storage, built by ...

Result # 3 Relevance: ○

Prefetching for a Chain of Control Blocks

1993-03-01 IPCOM000104183D English (United States)

Prefetching for L1-CACHES that are preformed by an L2 cache using a mechanism based on information derived from the processor at the time of the L1-D-CACHE miss. The amount of information can be extended to include the instruction image, that caused the miss, and thereby ...

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Result # 1 Relevance: ○○○○○

Decode Compound Checker

1993-08-01 IPCOM000105647D English (United States)

In a typical SCISM processor, instructions are examined for parallel execution prior to instruction decode, for example during cache-miss processing. Instructions identified for parallel execution are called a compound instruction. This information is stored with the ...

Result # 2 Relevance: ○○○○

Cache Miss Director - A Means of Prefetching Cache Missed Lines

1982-08-01 IPCOM000050035D English (United States)

In a computing system with a cache, when the CPU encounters a storage reference that cannot be satisfied by the cache (a demand miss), processing usually must be delayed for an access to main storage. Because of the increasing disparity between CPU and main storage speeds, ...

Result # 3 Relevance: ○○○

Method for a consecutive events predictor for future low-power techniques in very high performance microprocessors

25-Feb-2002 IPCOM000007094D English (United States)

Disclosed is a method for a consecutive event period predictor for low-power techniques in very high performance microprocessors. Benefits include improved system performance and improved power utilization.

Result # 4 Relevance: ○○○

Biasing Cache Threshold Pointers Toward Less Pre-Staging

1989-01-01 IPCOM000034301D English (United States)

A technique is described whereby computer cache storage performance is improved by biasing cache threshold pointers toward less pre-saging. The concept adjusts the threshold pointers so that when the hit ratio varies little, or not at all, over the entire range of threshold ...

Result # 5 Relevance: ○○○

Improving File Retrieval Performance in Content Manager

2004-09-10 IPCOM000031108D English (United States)

IBM DB2 Content Manager(CM) provides a common interface for managing content. A typical CM configuration includes a library and one or more resource managers. System Administrator can assign a user's default Resource Manager(RM) as a LAN cache server. A LAN cache server ...

Result # 6 Relevance:

Method for stride-profile guided prefetching for irregular code

16-Jun-2004 IPCOM000029128D English (United States)

Disclosed is a method for stride-profile guided prefetching for irregular code. Benefits include improved functionality and improved performance.

Result # 7 Relevance:

Method for Aggressive Function Cloning and Embedding with Global Code Reordering

2004-12-06 IPCOM000033308D English (United States)

Given a program code along with profiling information about the frequency of its instructions, gathered with some representative workload, the proposed method produces optimized code with improved performance.

Result # 8 Relevance:

Staging Length Table - A Means of Minimizing Cache Memory Misses Using Variable Length Cache Lines

1982-08-01 IPCOM000050034D English (United States)

In a computing system with a cache, when the CPU encounters a storage reference that cannot be satisfied by the cache (a demand miss), processing usually must be delayed for an access to main storage. Because of the increasing disparity between CPU and main storage speeds, ...

Result # 9 Relevance:

A Unified and Flexible Priority Scheme for Controlling a Write Buffer

2001-11-20 IPCOM000005969D English (United States)

Next generation portable devices are placing stringent requirements on overall system power and performance. Voice recognition, streaming video and high speed wireless internet access are just some of the features being incorporated in these handheld electronic gadgets. ...

Result # 10 Relevance:

Demand Driven Instruction Fetching Inhibit Mechanism

1980-07-01 IPCOM000055476D English (United States)

Disclosed is a technique that minimizes damaging contention for access to a high speed storage (cache) during line transfer operations. This is accomplished by means of a hardware mechanism which dynamically determines when to inhibit a hardware conditional ...

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Search query: cache miss AND threshold

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